



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,513	04/20/2001	Paul F. Struhsaker	WEST14-00033	2906
7590	01/09/2004		EXAMINER	
William A. Munck, Esq. NOVAKOV DAVIS & MUNCK, P.C. 900 Three Galleria Tower 13155 Noel Road Dallas, TX 75240			PHAN, RAYMOND NGAN	
			ART UNIT	PAPER NUMBER
			2111	6
			DATE MAILED: 01/09/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,513	STRUHSAKER ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
 5) Claim(s) ____ is/are allowed.
 6) Claim(s) 1-8 and 12-18 is/are rejected.
 7) Claim(s) 9-11,19 and 20 is/are objected to.
 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on ____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4,5</u> . | 6) <input type="checkbox"/> Other: _____ |

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-20 are pending.
2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 12-14, 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over DeYesso et al. (US No. 5,371,743) in view of Kim et al. (US No. 6,253,267).

In regard to claims 1, 12, DeYesso et al. disclose the use in association with a backplane of the item of electronic equipment wherein the backplane comprising a common control bus 15 that can access a first number of device locations, an

Art Unit: 2111

apparatus capable of allowing the common control bus to access more than one first number of device locations (see figure 1, col. 3, line 17 through col. 4, line 37). But DeYesso et al. do not disclose the apparatus comprising a complex programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the complex programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus. However Kim et al. disclose programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus (see col. 3, lines 7-49). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 2, Kim et al. disclose wherein the complex programmable logic device controls the access of a device to the common control bus when a device location of the device is coupled to the common control bus (see col. 3, lines 7-49). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claims 3, 13, Kim et al. disclose wherein the complex PLD coupled to device location the circuit board card to the common bus control to allow the common control bus to access a second number of device locations on the circuit board card through the complex PLD (see col. 3, lines 7-49). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 4, 14, Kim et al. disclose wherein the second number of device locations on the circuit board card that the common control bus can access through the complex PLD is greater than the first number of device locations that the common control bus can otherwise access (see col. 3, lines 7-49). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 18, DeYesso et al. disclose the use in association with a backplane of the item of electronic equipment wherein the backplane comprising a common control bus 15 that can access a first number of device locations, an apparatus capable of allowing the common control bus to access more than one first number of device locations (see figure 1, col. 3, line 17 through col. 4, line 37). But DeYesso et al. do not disclose the apparatus comprising a complex programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the complex programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling

each one of the plurality of device locations on the circuit board card to the common control bus. However Kim et al. disclose programmable logic device (i.e. PLD) on the circuit board within the backplane, wherein the programmable logic device is coupled to the common control bus, and wherein the complex programmable logic device is capable of coupling each one of the plurality of device locations on the circuit board card to the common control bus (see col. 3, lines 7-49); receiving data in the PLA through the signal bus line (see col. 2, line 62 through col. 3, line 49); interpreting instructions in the data to allow PLA to control data access to the first device (see col. 2, line 62 through col. 3, line 49). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Kim et al. within the system of DeYesso et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

6. Claims 5-8 and 15-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over DeYesso et al. in view of Kim et al. and further in view of Ptasinski et al. (US No. 6,363,437).

In regard to claim 5, DeYesso et al. and Kim et al. teach the claimed subject matter as discussed above except the teaching of a card processor (i.e. controller) on the circuit board card within the back plane, the card processor coupled to the common control bus (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 6, Ptasinski et al. disclose wherein the card processor is coupled to the common control bus through the serial clock line (SCL) and through the serial data line (SDL) connection (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claims 7, 17, Ptasinski et al. disclose further comprising the EEPROM on the circuit board card coupled to the common control bus; wherein the complex PLD controls the access of EEPROM to the common control bus when the EEPROM is coupled to the common control bus (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 8, Ptasinski et al. disclose wherein the EEPROM is coupled to the common control bus through the serial clock line (SCL) and through the serial data line (SDL) connection (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 15, Ptasinski et al. disclose further comprising the step of coupling the card processor on the circuit board card within the back plane to the common bus; providing clock signals to the card processor from the serial clock line coupled to the common data bus; reading data from the card processor on the serial data line coupled to the common data bus; and writing data to the card processor from the serial data line (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

In regard to claim 16, Ptasinski et al. disclose further comprising the step of coupling the EEPROM on the circuit board card within the back plane to the common bus; providing clock signals to the EEPROM from the serial clock line coupled to the common data bus; reading data from the EEPROM on the serial data line coupled to the common data bus; and writing data to the card processor from the serial data line (see figure 7A, col. 3, lines 47-62). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Ptasinski et al. within the system of DeYesso et al. and Kim et al. because it would reduce the costs and increase reliability by implementing all functions for the hot plug on a single chip.

Allowable Subject Matter

7. Claims 9-11, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2111

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 9-10 and 19 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach the complex PLD is coupled to the common control bus through the serial clock line (SCL) and through the serial data line (SDL) connection (claim 9); the common control bus comprising a first two wire bus and a second two wire bus and wherein the card processor, EEPROM and complex PLD coupled to the first two wire bus and to the second two wire bus through the MOSFET switches (claim 10); the step of interpreting in the complex PLD a first portion of a first byte of the data to identify the card address of the first device; second portion of the first byte of the data to identify a device code of the first device and the third portion of the first byte of the data to identify an instruction to read data or to write data to the first device (claim 19).

The remaining claims, not specifically mentioned, are allowed for the same reason as set forth parent claims 10 and 19.

Conclusion

9 Claims 1-8 and 12-18 are rejected. Claims 9-11 and 19-20 are objected.

10. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Hill et al. (US No. 6,209,051) disclose a method for switching between multiple hosts.

Matsuoka (US No. 6,009,492) discloses an expansion device and computer system to which expansion device can be connected.

Chen et al. (US No. 6,591,324) disclose a hot swap processor card and bus.

Van Krevelen et al. (US No. 6,230,229) disclose a method and system for arbitrating path contention in a crossbar interconnect network.

Papa et al. (US No. 6,418,492) disclose a method for computer implemented hot swap and hot add.

Comfort et al. (UK No. 2,195,028A) disclose a testing electrical circuits.

Son (US No. 6,233,635) discloses a diagnostic/control system using a multi-level I2C bus.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Raymond Phan 
1/7/04